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Intel® 915GMS Chipset: In Mobile Platforms, Smaller is Better

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Intel® 915GMS Chipset: In Mobile Platforms, Smaller is Better

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ABSTRACT

The Intel® Centrino™ mobile technology is based on four basic vectors of mobility: breakthrough mobile performance, integrated Wireless LAN (WLAN) capability, great battery life, and thinner, lighter designs. Historically, Intel's focus has been on increasing performance and, to a lesser extent, on improving power consumption. Intel Centrino mobile technology sharpens this focus and also allows Intel to increase the feature set of the platform to include wireless solutions. In this paper, however, we focus on the mostly overlooked promise of the fourth vector of mobility: thinner, lighter designs.

The packaging, manufacturing, and motherboard routing issues associated with enabling thinner lighter designs are explored in detail. We discuss the package electrical and motherboard breakout challenges, exploring the ideas and concepts used to ensure that reducing the package size will allow for high-volume manufacturing requirements. Finally, we discuss how Intel enables unique form factors through the support of specialized motherboard routing techniques. All of these solutions allow Intel Centrino mobile technology to provide a very convincing answer to the challenge of innovating compelling form factors.

INTRODUCTION

The Intel Centrino mobile technology was specifically developed for on-the-go computing, with a focus on the four vectors of mobility: breakthrough mobile performance, integrated Wireless LAN (WLAN) capability, great battery life, and thinner, lighter designs. When Centrino mobile technology platforms were introduced in March of 2003, notebooks became much smaller (X and Y) and much thinner (Z) compared to previous notebooks based on the Intel Pentium® 4 processor. This reduction was primarily due to the significantly lower Thermal Design Power (TDP) of the processor and the Graphics and Memory Controller Hub (GMCH) components compared to previous platforms.

However, even smaller form factors could not be developed as the size of the processor and GMCH components was still quite large; in fact these components were the largest two components on a mobile motherboard. For example, the Intel 855GM GMCH package was 37.5 mm square, even though the silicon die size was only 9 mm square. This was due to the very large number of pins on the package together with the board assembly technology required to get all these signals routed onto the motherboard.

As Intel started to develop the next-generation mobile PC platform built on Intel Centrino mobile technology, the GMCH package size actually grew by 7% to 37.5 mm x 40 mm. This growth was primarily due to the addition of a second channel of Double Data Rate (DDR2) system

memory, that was required for the highest performance mobile notebooks. In order to continue to drive the thinner, lighter designs vector of mobility, Intel wanted to develop a significantly smaller GMCH package, specifically designed for the smallest (X and Y) and thinnest (Z) systems. Thus the idea of the Intel 915GMS chipset was born.

This paper explains the steps Intel took to design this new product. We first explain how the number of signal and power pins was reduced on this product, and how the package ball pitch was optimized while maintaining effective board routing. Second, we address the manufacturing concerns that result from a significantly smaller package. The result of our work was the creation of a 27 mm square Intel 915GMS package, a 51% size reduction from the standard Intel 915 package.

Third, we explain additional board-routing guidelines that were developed to allow mobile Original Equipment Manufacturers (OEMs) to further compress their motherboard layout. It is hard to know what new form factors will result from this, but OEMs are very creative when it comes to smaller and sleeker notebooks. We end with some ideas on what new usage models might result from this work, and we discuss future challenges for the continued push toward compelling form factors.

INTEL 915GMS BREAKOUT ROUTING CHALLENGES AND SOLUTIONS

The standard Intel 915 chipset was developed in a 37.5 mm x 40 mm package. Many techniques were used to reduce the size of the Intel 915GMS package while still meeting the needs of the small form factor market.

Interface Removal

One of the easiest ways to reduce the size of a package is to remove unnecessary features. A detailed investigation of the small form factor market led to an understanding of what subset of features of the Intel 915 chipset were needed. As seen in Table 1, ~300 pins were removed on four key Intel 915GMS interfaces.

Table 1: Pin-reduction summary

Interface	915GM	915GMS	# Removed
PCIe to Ext.GFX	142	32	110
DDR to Memory	383	227	156
DMI to ICH	35	18	17
LVDS to Panel	41	25	16

During this analysis we found that the small form factor segment does not typically have room to accommodate an external graphics controller and therefore is primarily designed for internal graphics. Since the Intel 915 chipset family supports both internal and external graphics configurations, external graphics support was removed from the Intel 915GMS product in order to eliminate the majority of the Peripheral Component Interconnect (PCI) Express* interface and its associated signal pins. This allowed us to remove 50 signal pins and 60 ground pins.

Another thing we found was that most of the small form factor systems only require a single channel of memory support due to their reduced performance needs. Since the Intel 915 chipset family supports both dual-channel and single-channel system memory, one of the two channels was removed to save ~120 signal pins. This also allowed approximately 30 power pins to be removed since fewer power pins were needed to support a single-channel memory configuration.

In addition to the reduced memory performance requirements, it was found that the small form factor systems also have reduced I/O performance requirements. The Intel 915 chipset family supports both a 4-lane Direct Media Interface (DMI) and a 2-lane DMI between the GMCH and the I/O Controller Hub (ICH). The reduced I/O performance requirement of the small form factor segment allowed us to alter the DMI bus for this chipset to only support a 2-lane configuration, and we thus were able to remove 17 more pins.

Finally, we found that most of the small form factor LCDs selected by OEMs and Original Design Manufacturers (ODMs) utilize a single channel of Low Voltage Differential Signaling (LVDS). This finding allowed the design team to remove one of the LVDS channels when developing the Intel 915GMS chipset to save another 16 pins.

The removal of these pins associated with the unnecessary interfaces allowed for a major reduction in package size, resulting in a 31 mm x 31 mm package. We then moved on to investigate making pin pitch changes to the pinout in order to shrink the package size even further.

Parquet Package Technique

The standard Intel 915 chipset product utilizes a uniform grid pin pitch of 42 mils. This pin pitch was selected to allow two traces to route between the via field in the breakout region, assuming a via antipad diameter of 30 mils (a via size typically used in mobile high-volume manufacturing). After the vias' antipad area is accounted for there is only 12 mils of remaining room for trace routing. As illustrated in Figure 1, utilizing a standard

* Other brands and names are the property of their respective owners.

stripline trace width of 4 mils allows for two traces to fit between the vias with 4 mils of space between them (hereafter referred to as 4:4 routing).

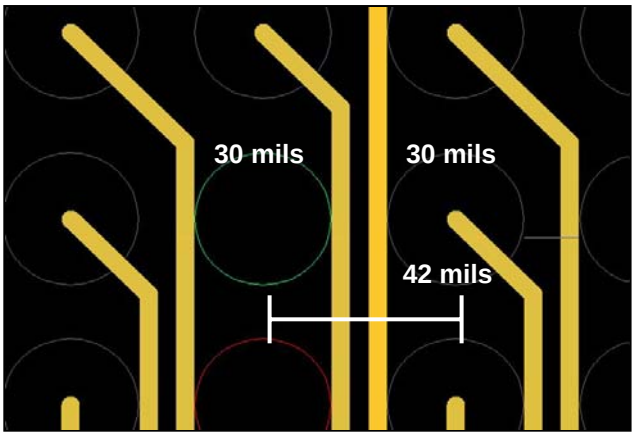

Figure 1: Breakout region routing dictated by via size

As can be seen, the minimum allowable pin pitch is directly related to the via size that is assumed for the platform. For the majority of mobile designs the standard via uses an antipad size of 30 mils so the resulting pin pitch is 42 mils (to allow for two tracks of 4:4 routing). However, the analysis of the small form factor market segment showed an inclination to utilize slightly more expensive motherboard technologies. This analysis showed that a 28 mil antipad was acceptable in this market and would allow for some pin compression. Therefore, the Intel 915GMS pin pitch was reduced from 42 mils to 40 mils (assuming a via with a 28 mil antipad).

Upon closer inspection of the breakout routing of the standard Intel 915 chipset package, it was determined that the perpendicular (or "transverse") routing channels were not being utilized. In effect, all of the signals were breaking out in a radial fashion away from the center of the package. This observation led to the idea of reducing the perpendicular pin pitch to something smaller than 40 mils to "compress" the package even further. In order to achieve an equal amount of compression along all four package sides, the parquet technique was developed.

The parquet package technique is composed of four periphery sections and a center region. Each of the periphery sections utilizes a wider pin pitch in the direction along the package edge, and they utilize a reduced pin pitch in the direction towards the package center (see Figure 2). The result is a 40 x 32 mil parquet pin pitch.

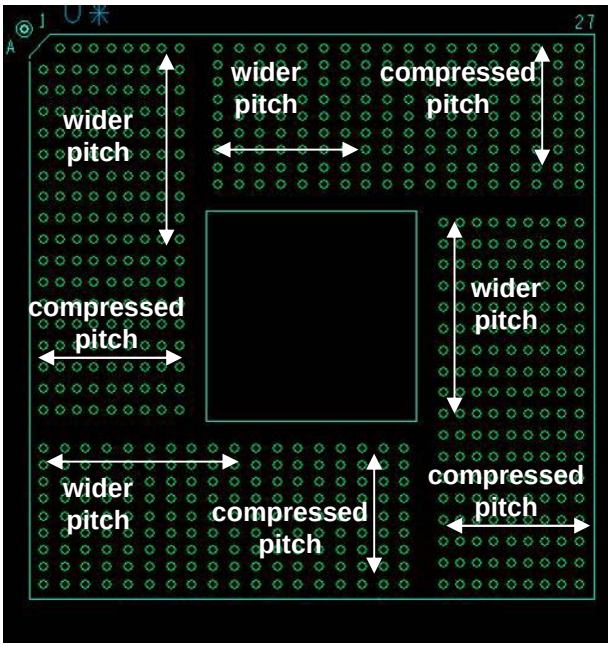

Figure 2: Parquet package illustration

The parquet package routing technique is not without challenges of its own. In particular, since one of the pin pitches is reduced to 32 mils, there is only enough room to route one signal in a perpendicular fashion to the typical breakout direction. This in itself presents no problem, because as the signal density increases so can the complexity of trying to find a breakout routing solution for each of the signals (see Figure 3).

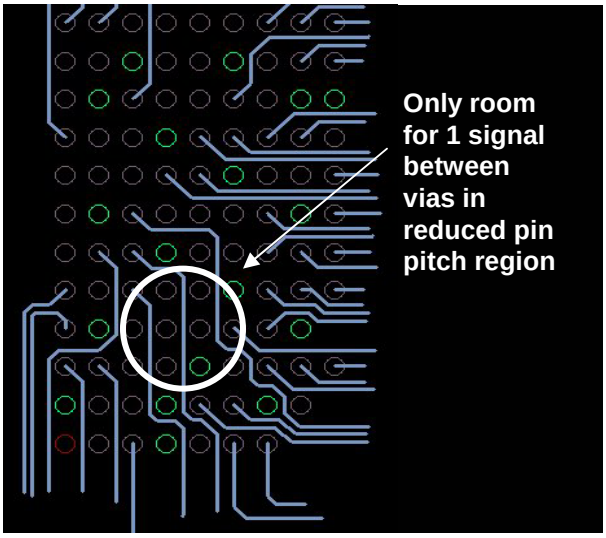

Figure 3: Transverse parquet routing

Corridor Routing

An additional benefit of the parquet package technique is that it provides natural "gaps" or "corridors" where two different parquet periphery sections meet. These corridors

have a wider pin pitch and therefore can be used to route more signals, or to provide a wider gap for power delivery (see gaps between periphery sections in Figure 2).

In addition to the natural corridors, the Intel 915GMS pinmap creates some artificial corridors with power pin assignments. The pinmap assigns power pins in corridor shapes from the edge of the package towards the center region. These "power corridors" have power delivery benefits since they allow a wider copper flood on the surface layer to connect to the package and therefore can accommodate higher currents and provide a lower DC-power loss routing path for power delivery (see Figure 4).

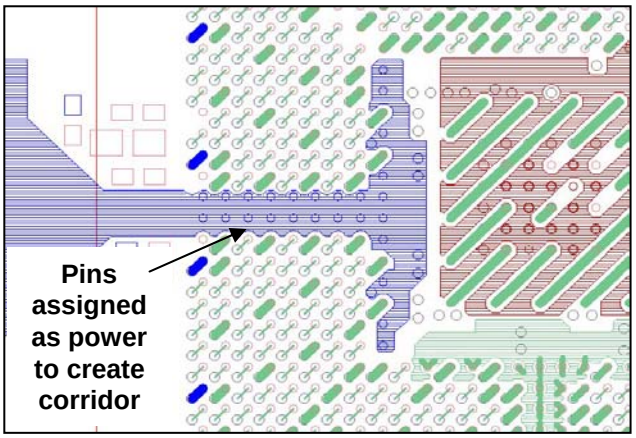

Figure 4: Power corridor on top-surface layer

Another benefit of the corridors is that they allow higher signal density breakout on the inner stripline layers due to that region being absent of vias. Without a via being associated with every package pin, these corridors can be seen on internal routing layers as a wide unused region through which many signals can be routed. This allows for greater signal density within a smaller package size (see Figure 5).

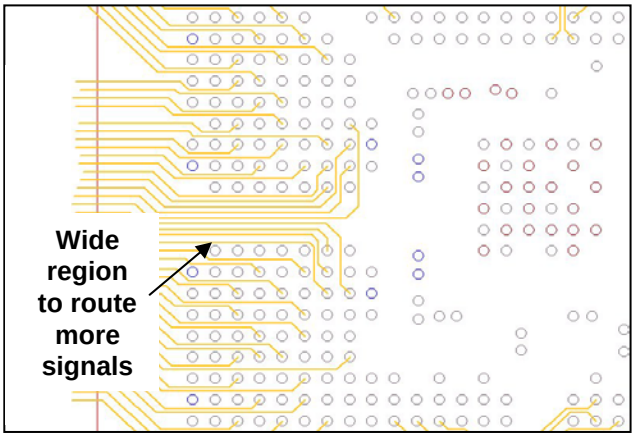

Figure 5: Signal routing under power corridor

The final benefit of power corridors is that the same advantage seen on internal layers is seen on the backside surface layer. Just like the wide open regions on the internal layers, the backside surface layer is open and can be used to deliver wide copper floods for additional power delivery (see Figure 6).

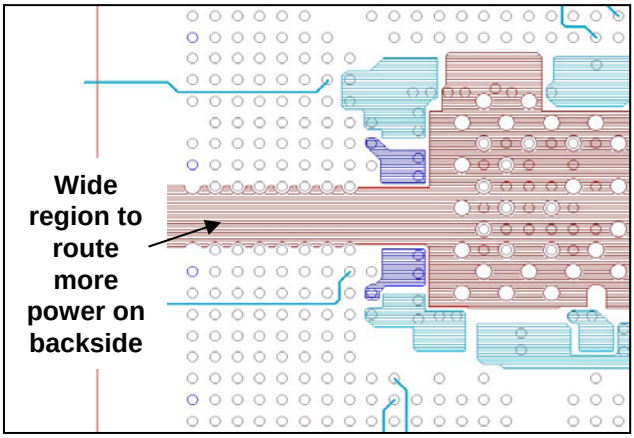

Figure 6: Power routing under power corridor

Together with interface removal, the parquet package technique, and corridor routing, the size of the Intel 915GMS package was reduced to 27 x 27 mm, a 51% area reduction from the original 37.5 x 40 mm package size of the standard Intel 915 chipset.

PACKAGE SUBSTRATE LAYOUT AND PACKAGE TECHNOLOGY CHALLENGES

The challenges faced by the package development team in delivering the Intel 915GMS package included pushing key assembly technology parameters.

Package Size and Layer Stack-up

The package development team was given the task of delivering the smallest package possible for the given product feature-set yet still meeting the electrical requirements.

Using a 6-layer package substrate, similar to the standard Intel 915 chipset package, would have resulted in a package size of at least 35 mm. Moving to an 8-layer package substrate would enable the bulk of the signals, mainly front-side bus (FSB) and DDR2, to be routed as striplines, and this would reduce the size of the package. As mentioned earlier, there were a couple of package sizes that were considered during the feasibility analysis phase.

Refer to Figure 7 and Figure 8 for definitions of microstrip and stripline routing.

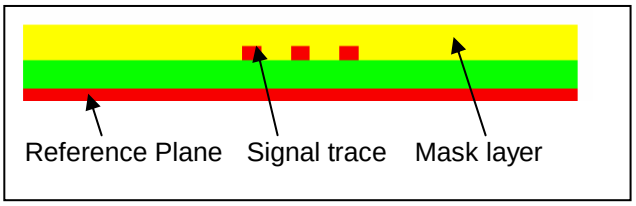

Figure 7: Microstrip signal routing

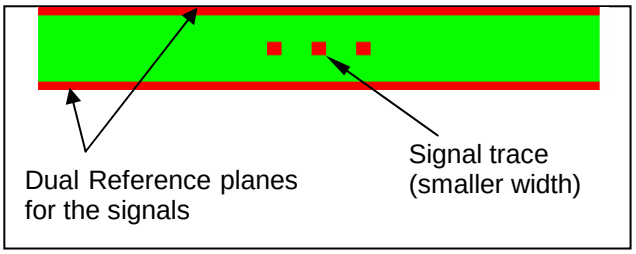

Figure 8: Stripline signal routing

The Intel 915 chipset used a 6-layer package substrate with all the signals routed on the surface layer as microstrip. Stripline routing with smaller trace width and spacing, when compared to microstrip routing, allowed us to achieve more routes per unit area, while maintaining the electrical integrity. Utilizing a 26 µm trace width for stripline results in a 50-ohms impedance as compared to a 55-ohm impedance which is found on the Intel 915 chipset. We decided to proceed with a 26 µm trace width for FSB and DDR2. The 5-ohms mismatch was deemed a non issue for FSB speeds @ 400/533 MHz. With DDR2 motherboard routing optimal at 40-ohms, the 50-ohms on the Intel 915GMS package was seen as an advantage over the 55-ohms on the standard Intel 915 chipset package.

Sub 1.0 mm Ball Pitch

One of the two package options required a minimum ball pitch of 0.8128 mm (32 mils) that was falling out of the Intel certified flip chip package technology envelope. Limited experimental reliability data was available on sub 1.0 mm ball pitch. The initial experimental data collected for the shock and vibrations test, for sub 1.0 mm ball pitch, showed that the solder joint reliability was a manageable risk. The product development team decided to continue working on the sub 1.0 mm pitch package design.

The package substrate design was intercepted, just before the design completion, to enlarge the ball grid array (BGA) pad size, an increase that was recommended based on the initial experimental results. For the subsequent shock and vibration experiments, Design of Experiments (DOEs) were planned with refined mobile shock tests and increased pad size on the substrate. Engineers from the Intel Technology and Manufacturing groups and the Mobile Chipset Products group worked closely to define a new experimental set-up including the Shock-Test Board design and the revised Shock-Test Spec. Interaction with key customers to understand the system-level designs and their capability for shock and vibration formed part of the DOEs' planning process. The data collected using the Intel 915GMS chipset Thermo-Mechanical Test Vehicle (TMTV) showed that the overall shock and vibration risk level of the Intel 915GMS package was manageable, and so the technology was certified.

Keep-Out Zone (KOZ) Reduction

Certain areas on the top surface of the package must be clear of any interferences: the die, decoupling capacitors, and underfill material. These are called Keep-Out Zones (KOZs) and are needed for handling of the package during the package assembly and testing processes.

Figure 9 shows the KOZs surrounding the die and the package periphery. The zones shown were defined as per the Intel Package Design specifications. As you can see, there is an overlap of KOZs at various locations. The overlapping of the KOZs violated the design specification and does not accommodate any on-package capacitors.

Experiments in the assembly and test areas were initiated to determine how to reduce the KOZs. The experiments yielded positive results. The Edge exclusion zone was reduced by over 25% of the specification and the Corner exclusion zone was reduced by 35%.

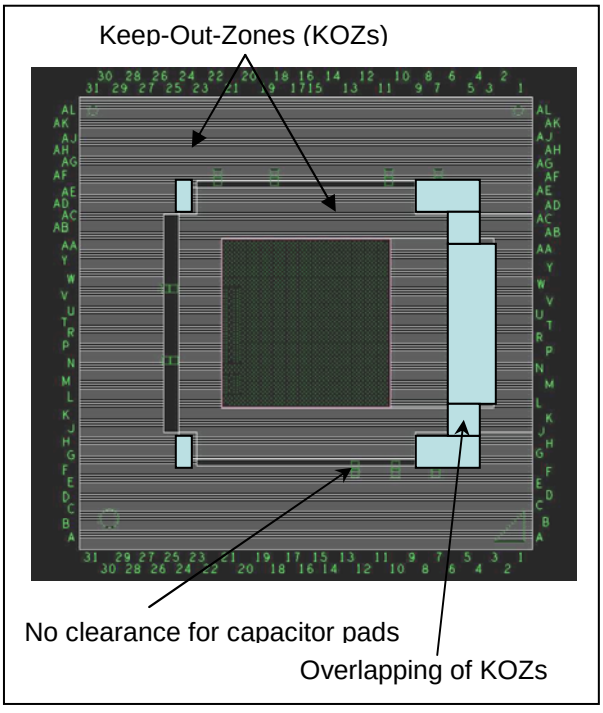

Figure 9: KOZs overlapping (before modifying the Intel Package Design spec)

Figure 10 shows the modified KOZs, which allowed the design to accommodate the on-package capacitors.

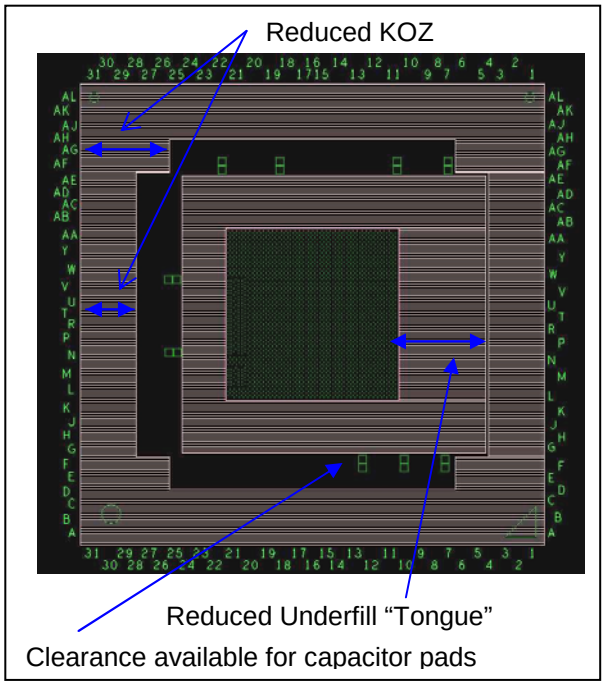

Figure 10: KOZs after modification of Intel Package Design spec

Also, the assembly line experiments showed that we could reduce the Underfill Tongue-width by 17%, which was needed to avoid overlap with the already "reduced" edge exclusion zone. A "trench" was cut on the top solder mask layer that further enabled us to reduce the tongue width. Since the routing on the east side was stripline, the trench was implemented without any signal traces passing across the trench. Figure 11 shows the trench design.

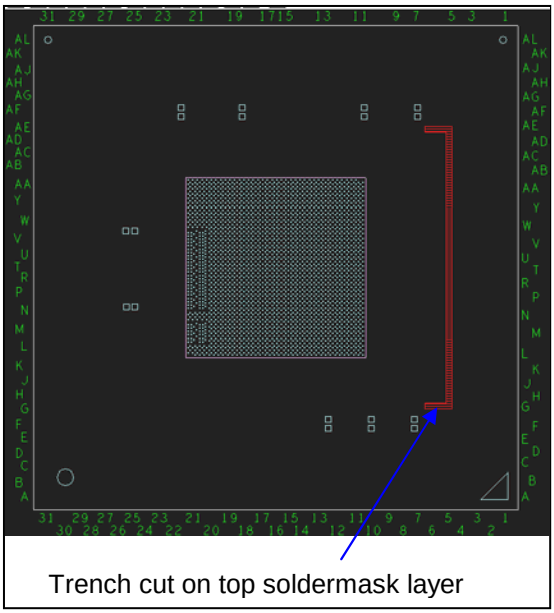

Figure 11: Location of the trench

MOTHERBOARD ROUTING IMPROVEMENTS

Along with providing an optimized chipset for small form-factor platforms, Intel has also put effort into developing guidelines to help in reducing the motherboard size and in reducing the effort required to design a small form-factor platform.

In the following sections, we discuss these guidelines and their benefits. The guidelines are optimized for two important areas: system memory and FSB.

System Memory Guidelines

With the Intel 915GMS chipset, Intel provided guidelines for implementing on-board memory that helps to reduce the size of the board. In a notebook design, there are many benefits if one can design the memory on the board rather than utilizing Small Outline Dual Inline Memory Modules (SO-DIMMs). By going for on-board memory, along with a reduction in the board size, a reduction in height can also be achieved.

Typically, the notebooks that are available in the market have two SO-DIMM slots. The product is sold with one SO-DIMM pre-installed; if consumers wish to increase the memory, they can buy an additional SO-DIMM and upgrade their notebooks. With Intel 915GMS platforms, designers can take advantage of the new on-board memory guidelines to change the pre-installed memory from SO-DIMM to on-board memory. Also, with products where a memory upgrade by the end user is not feasible, on-board memory can supply the total memory requirements of the platform.

Figure 12 illustrates the benefits achieved, with respect to board size and height, when designed with one SO-DIMM and on-board memory as compared to two SO-DIMMs. Benefits would even be greater if only on-board memory is supported.

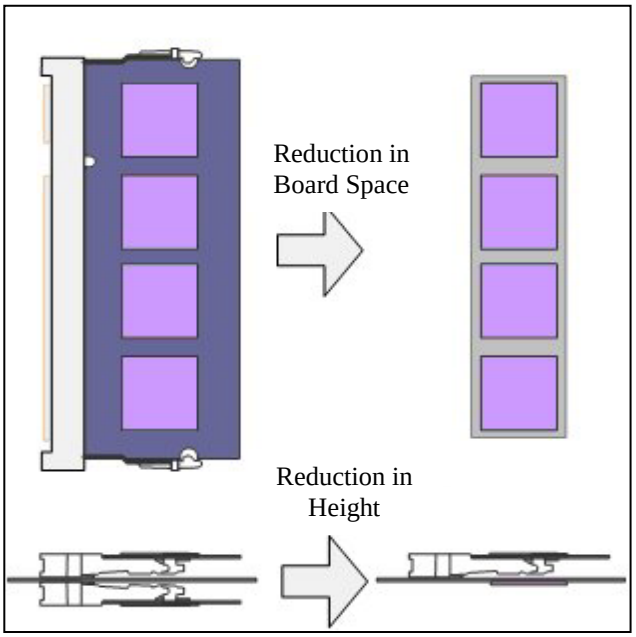

Figure 12: Benefits of on-board memory

Intel provides guidelines for various configurations with SO-DIMM and on-board memory. With these configurations, one can design the platform that can support up to 2 GB of memory. Table 2 lists these configurations and the maximum memory possible when 1 Gbit memory devices are used.

Table 2: Various configurations

Configuration (in space-saving order)	Max Memory (with 1 Gbit Technology)
1 rank (4 devices) on-board	512 MB
2 ranks (8 devices) on-board	1 GB
1 SO-DIMM	1 GB
1 SO-DIMM & 1 rank on-board	1.5 GB
1 SO-DIMM & 2 ranks on-board	2 GB
2 SO-DIMMs	2 GB

A configuration of four SDRAM components, where all four components are on the same side in one row, is the simplest configuration to route and yields the best signal integrity as well as timing budgets. When designing with eight SDRAM components, it is recommended to have four components on the top and four on the bottom of the board. This configuration is easier to route and has better signal integrity than designs where all of the eight components are on the same side: these may necessitate the use of more than 8-layer boards in order to route all of the memory signals.

For the configurations with on-board memory, the recommendations are for the SO-DIMM to be placed closest to the Intel 915GMS and the on-board memory SDRAM devices to be placed farthest away from the Intel 915GMS. Figure 13 shows the topology for one SO-DIMM and eight devices on the board.

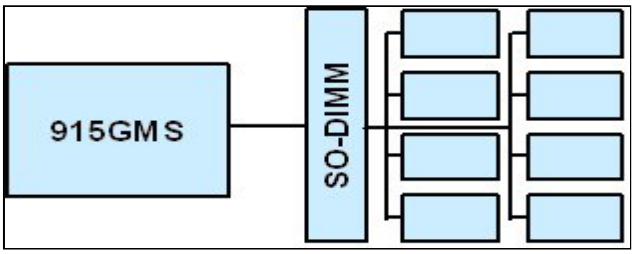

Figure 13: Simplified topology with eight memory devices

Front-Side Bus Guidelines

Intel 915GMS supports a 400 MT/s FSB to connect to low-voltage and ultra-low-voltage processors based on Intel Pentium M 90nm technology. The FSB guidelines were optimized to ease the routing on small form-factor platforms. With these optimized guidelines, the minimum routing length of the FSB signals can be as low as 0.1" as compared to 0.5" for earlier platforms. This provides the possibility of placing the processor and the Intel 915GMS very close to each other. Also, the minimum signal-to-signal spacing of the FSB interface can be as low as 1:1 (4 mil trace and 4 mil space) as compared to 1:2 (4 mil trace and 8 mil space) of earlier platforms. The reduced spacing requirement makes routing of FSB signals more flexible and also allows for denser routing of the signals. This leads to a reduction in the required routing space on the board.

INTEL 915GMS USAGE MODELS

Up to this point we have focused our discussion on what was done to reduce the size of the Intel 915GMS chipset. This reduced size delivers on the Intel Centrino brand promise of enabling unique form factors. However, what exactly will these products look like? How can this technology be used?

There are many vertical segments that might be interested in smaller and lighter form factors: health care, research, entertainment, and education, for example. These designs could be in the form of Tablet PCs, extremely thin-and-

light notebooks, or something radically new. Only time will tell what creative OEMs will do with these platforms, based on the Intel 915GMS platforms.

In the field of health care, for example, people move around a lot such as in hospitals where doctors and nurses need to gather information from many patients. Most of this information today is not digitized. Smaller tablet designs could provide the right combination of features to push digitization into this field and make this usage model real.

Similar to the health care profession, researchers in all disciplines require mobility in order to collect information in the field. For these individuals, smaller and lighter notebooks would provide greater ease of data collection. Notebooks, based on the Centrino mobile technology, also provide the ability to wirelessly upload these data to laboratories for analysis and storage.

OEMs targeting consumers who purchase mobile PCs to enjoy entertainment have many opportunities to take advantage of smaller form factors. The reduced size of the Intel 915GMS could be coupled with designed-in features like small wide-aspect ratio LCDs, and the capability to instantly wake-up the platform into a DVD-playback mode. This effort could result in a smaller entertainment focused mobile platform.

As notebook computers get smaller and lighter, their use in education by students will also increase. For example, students currently carry most of their text books to and from school. By making use of Intel's smaller and lighter notebooks, students would have less heavy books to carry; something that would also make it easier for younger students where the weight of books is often an issue.

As the market for personal computers expands so will the demanded usages from customers. The examples listed above are only a few of the areas where the Intel 915GMS chipset can provide for further development of the uniqueness that mobility provides.

Future Challenges

The Intel 915GMS chipset improves upon the form-factor promise of the Intel Centrino mobile technology brand. However, there are areas where future improvements could be made in order to allow form factors to become even smaller. The underlying design challenge is to reduce the size of the platform, while still providing performance and great battery life.

First and foremost, the techniques used on the Intel 915GMS product need to be utilized on other components on the platform, including the Intel Pentium M processor, ICH, and wireless solutions. Ball pitch and board routing technologies can be pushed to even further reduce package sizes. And additional integration of other platform components, removal of resistors and capacitors, and voltage plane reduction will all help to even further reduce the size of systems based on Intel Centrino mobile technology.

Advancement in some of these areas will be required to continue to push the vector of thinner, lighter designs, and some are being considered by Intel for use in future generations of small form-factor designs.

SUMMARY AND CONCLUSION

Together with signal and power-pin reduction, optimized package ball pitch, and resolution of manufacturing concerns, Intel was able to develop the Intel 915GMS product with a 27 mm square package, a 51% reduction from the standard Intel 915 package.

The excitement from the customer base is clear: there are more than a dozen Intel 915GMS platforms in development, all ready to launch in the March 2005 through September 2005 timeframe. Customers will be able to take advantage of this small package, and use the routing guidelines to further reduce the board area of their products. Intel expects that this will enable smaller and sleeker form factors, and potentially new usage models. And as the interest of platforms based on Intel Centrino mobile technology continues to grow, it is clear that the Intel 915GMS is just the first of many products focused on smaller and sleeker form factors.

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